Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 7. This sheet, which includes Fig. 7 replaces the original sheet including Fig. 7.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS/ARGUMENTS

The undersigned called the Examiner on June 26 to discuss Figure 7. During the call, it was respectfully brought to the attention of the Examiner that element 410 refers to PCI-X or 3GIO card, and element 420 refers to host mainboard 42, disclosed in paragraph 37 of the original disclosure. Accordingly, the Examiner agreed to withdraw objections number 1 and 3 to the drawings.

Claims 1-15 remain pending in this application and stand rejected. Claims 1 and 9 are amended, in part, to clarify their respective languages and more fully define the scope of the inventions claimed therein. For example, claim 1 is amended to recite, in part, "an image processing engine adapted to perform object-independent processing .... to generate a first set of processed data; and a post processing engine adapted to directly receive the first set of processed data and to perform object-dependent processing ..... on the received first set of processed data thereby to generate a second set of processed data". Support for claim 1 is provided, for example, in Figure 7, where image processing Engine (IPE) 200 is shown as being in direct communication with post processing engine (PPE) 50. Support for this amendment is also provided, for example, in paragraphs 21, and 39, of the original disclosure:

> "In accordance with the present invention, object-independent processing layer 105, may be mapped onto (i.e., performed by) a massively parallel processor (MPP) or systolic array (shown in Fig. 5), and the object-dependent processing layer 110, may be mapped onto a symmetric multi-processor system (SMP), a uniprocessor, or an MPP. In one embodiment, the MPP may be an image processing engine (IPE), and the SMP may be a post processing engine (PPE), as described further below. Fig. 7 is a simplified high-level block diagram of an image processing system 400, in accordance with one embodiment of the present invention. As seen from Fig, 7 and described in detail below, system 400 includes, in addition to other components, an IPE 200, and a PPE 500. It is understood that object-

> independent processing refers to processing of pixel data that have not been associated with any objects and object-dependent processing refers to processing of data that have been associated with objects." (paragraph 21)
>
> "IPE 200 sends the detected results to PPE 500....." (paragraph 37)

New claims 16 and 17 are added.

Claims 1-15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Juvinall (US Patent No. 5,214,713), hereinafter referred to as Juvinall, in view of Chen et al. (U.S. Patent No. 5,535,288), hereinafter referred to as Chen. Applicant respectfully traverses these rejections. Nonetheless, to expedite the prosecution of the instant matter, the claims have been amended above.

In rejecting claim 1, the Examiner refers to camera 48 of Fig. 1, and column 10, lines 3-23 of Juvinall, partly reproduced below:

> "Systolic processor array 96 (FIG. 5) hereinabove described embodies 1,152 one-bit processors, each of which operates on one pixel byte (eight bits) at one time. In a camera 48 that employs a CCD array 54 (FIG. 2) of 512x256 CCD sensing elements, as shown in FIG. 2, there are thus over 130,000 pixels available for analysis."

In other words, Juvinall processes 2 lines of data at a time and not one frame at a time, as required by claim 1: " said image processing engine further adapted to include a plurality of processors each associated with a different one of pixels of the image frame". Because in accordance with the present invention, the per-pixel processing performed by the image processing engine is carried out on a per-frame basis, (i) the processing operation can be pipelined to improve efficiency; and (ii) the entire frame view of the object is in the field of view. Claim 1 is thus allowable over Juvinall for at least this reason.

Moreover, in Juvinall, the data processed by the systolic array is first stored in the memory, and is thereafter retrieved from the memory by the data-dependent processor for further processing:

> "By controlling operation of these electronics, the master computer obtains pixel data from the camera and stores such data by pixel in memory, retrieves pixel data from memory and loads such data by pixel into the systolic array processor such that each of the plurality of one-bit processors receives and operates on one byte of pixel data, returns data from the systolic array processor to the memory, and retrieves pixel data from memory and loading such data into the data-dependent processor for non-sequential and/or data-dependent image processing." (Abstract)

In contrast, in claim 1, the data processed by the image processing engine is applied directly to the post processing engine without first storing this data in a memory, as recited, in part, in claim 1 "....a post processing engine adapted to directly receive the first set of processed data and to perform object-dependent processing". Because, in accordance with claim 1, data is supplied directly from the image processing engine to the post processing engine without being stored in the memory, no host CPU or DMA is involved, and the need to access a host DRAM is dispensed with. Accordingly, because Juvinall requires that the data processed by the systolic array be stored in the memory first before being retrieved from the memory by the data-dependent processor, Juvinall fails to teach or suggest claim 1 which recites, in part, "an image processing engine adapted to perform object-independent processing corresponding to a first layer of the image processing system to generate a first set of processed data....a post processing engine adapted to directly receive the first set of processed data and to perform object-dependent processing." Claim 1 is thus allowable over Juvinall for at least this additional reason.

As pointed out correctly by the Examiner, Juvinall also fails to disclose a post processing engine "adapted to include N-way symmetric multi-processing system (SMP) having

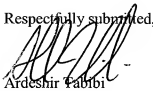
disposed therein N DFT engines and N matrix multiplication engine, wherein N is an integer greater than 1".

Contrary to the Examiner's assertions, Chen also fails to teach or suggest "a post processing engine adapted to directly receive the first set of processed data and to perform object-dependent processing corresponding to a second processing layer of the image processing system on the received first set of processed data thereby to generate a second set of processed data, said post processing engine further adapted to include an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1".

Applicant submits that there is no disclosure in Figures 5-7, and columns 7-9 of Chen of matrix multiplication. Furthermore, there is no disclosure in Figures 5-7, and columns 7-9 of Chen of "an image processing engine adapted to perform object-independent processing corresponding to a first layer of the image processing system to generate a first set of processed data, said image processing engine further adapted to include a plurality of processors each associated with a different one of pixels of the image frame; and a post processing engine adapted to directly receive the first set of processed data and to perform object-dependent processing corresponding to a second processing layer of the image processing system on the received first set of processed data thereby to generate a second set of processed data, said post processing engine further adapted to include an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1", as recited, in claim 1. Therefore, Juvinall, whether taken alone, or in combination with Chen, fails to teach or suggest claim 1. Claim 1 is thus allowable over Juvinall in view of Chen. Claims 2-8 and 17 are dependent from claim 1 and are thus allowable for at least the same reasons as is claim 1. Claim 9 and its dependent claims 10-16 are allowable over Juvinall in view of Chen for at least the same reasons as is claim 1.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (650) 752-2424.

Respectfully submitted,



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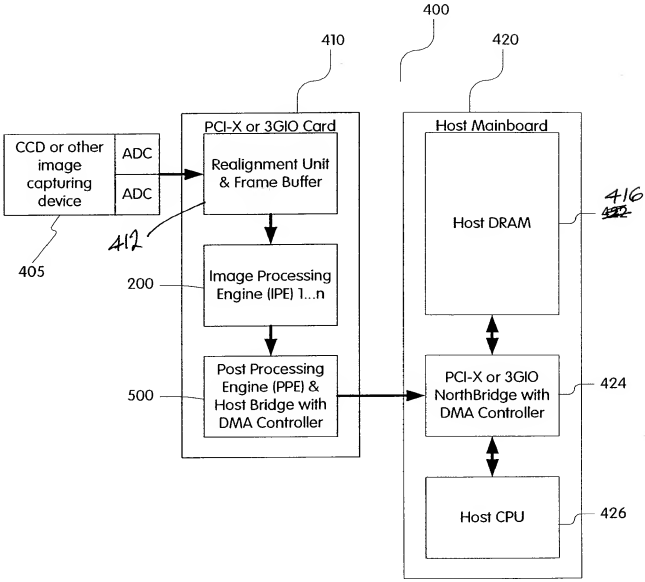
400
410
420
PCI-X or 3GIO Card
Host Mainboard
CCD or other image capturing device
ADC
ADC
Realignment Unit & Frame Buffer
412
405
Host DRAM
416
Image Processing Engine (IPE) 1...n
200
Post Processing Engine (PPE) & Host Bridge with DMA Controller
500
PCI-X or 3GIO NorthBridge with DMA Controller
424
Host CPU
426

Fig. 7